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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CAZAN, LIVIUS RADU	
ART UNIT	PAPER NUMBER
3729	

MAIL DATE	DELIVERY MODE
07/21/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,901	BUSCH, GEORG	
	Examiner	Art Unit	
	LIVIUS R. CAZAN	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10,13-17,19-24 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10,13-17,19-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. **Claim 26** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, there is no support in the specification for the limitation "wherein the electrically conductive layer is not coarsened between the steps of etching and applying an insulating layer". Simply because the specification is silent with respect to a particular feature does not provide support for a negative limitation completely excluding that feature. In manufacturing circuit boards there are many conventional steps involving washing, roughening of surfaces before lamination, the use of various chemicals in electroless and electrolytic plating, the use of photoresist, developer, and etchant in pattern transferring etc. Because such steps are well known, most often patent applications are silent with respect to some of the details, and, rather, focus on the main process steps. For example, a specification might state a metal layer is electroplated onto an insulating substrate. However, as is known in the art, an electroless metal deposition would be needed to form a thin conductive layer, so that current can pass therethrough during the electroplating. Simply because the

specification did not explain in detail how this electroplated metal layer is formed, this does not constitute support for claiming a metal layer electroplated onto a substrate without performing electroless deposition. In a similar manner, there is no support in the present application for excluding coarsening the electrically conductive layer.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 6-8, 13-15, 20-22 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose (US6407345), with Stopperan (US5719749) used as extrinsic evidence.

5. **Regarding claims 6, 8, 13, 15, 20, and 22**, Hirose discloses substantially the claimed invention, as previously discussed (see the Office Action mailed on 10/6/2008). With respect to the limitation "wherein the through-bores are approximately 20 μm in size", the Examiner has previously argued it would have been obvious to one or ordinary skill in the art to apply the method of Hirose to through-holes of the claimed size, depending on the particular design of the circuit, since the process steps are the same irrespective of the through hole diameter. As noted by Applicant, Hirose forms through holes with a radius of at least 125 μm, because it is difficult to form smaller holes by a drill. However, simply because Hirose was unable to drill smaller holes does not mean the process cannot be used with smaller through holes. Stopperan is provided as extrinsic evidence in support of the Examiner's position. In particular, Stopperan shows that it is known in circuit board manufacturing to form through holes via laser

drilling, which allows for holes smaller than 25 microns (i.e. approximately 20 microns; see col. 6, lns. 11-13). It is therefore readily apparent that the process of Hirose is not limited to the size of through holes disclosed by Hirose, but, rather, the process can be used with through holes of other sizes, including as claimed, as previously argued by the Examiner (see the Office Action mailed on 10/6/2008).

6. **Regarding claim 6**, no layers are applied to the circuit board between the steps of etching and applying an insulating lacquer.

7. **Regarding claims 7, 14, and 21**, Hirose discloses substantially the same invention as the Applicant, except for the medium used to fill the holes and the insulating lacquer being identical.

8. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to choose a medium and a lacquer suitable for the intended use, since this requires only routine skill in the art. As such, it would have been obvious for one of ordinary skill in the art to utilize the same material for the medium and the lacquer, if such a suitable material exists, because it is more economical to utilize a single material than to utilize two different materials.

9. **Regarding claims 13 and 20**, the lacquering is performed without brushing the electrically conductive general layer pf the circuit board.

10. **Regarding claim 26**, Hirose discloses substantially the claimed invention, except for not coarsening the electrically conductive layer between the etching and applying an insulating layer. See the above rejection under 35 U.S.C. 112, 1st paragraph.

11. While Hirose teaches coarsening the electrically conductive layer, it is readily apparent that the electrically conductive layer 32 laminated onto substrate 30 may already be provided with a roughness sufficiently high to not necessitate any further coarsening.

12. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to omit a step of coarsening the electrically conductive layer if it already possesses a sufficiently high roughness.

13. One of ordinary skill in the art would have been motivated to do so in order to speed up manufacturing time and reduce manufacturing cost by not performing unneeded steps.

14. **Claims 9, 10, 12, 16, 17, 19, 23, and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose as applied above in view of APA (Applicant's admitted prior art).

15. Hirose discloses substantially the same invention as the Applicant, except for the strip conductors being carbon, individual circuit boards being separated by milling, and the insulating lacquer being an International Standard Organization lacquer.

16. APA teaches that it is known to form carbon circuit patterns (step 8, page 5), to separate individual circuit boards by means of a milling process (step 10, page 5), as well as to use an ISO insulating lacquer (step 7, page 4) in manufacturing printed circuit boards.

17. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to apply these concepts in making the circuit board of Hirose, for the same advantages as when used in the prior art of APA.

Response to Arguments

18. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

19. Regarding Applicant's argument that Hirose teaches away from the claimed bore size, the Examiner respectfully disagrees. Applicant cites *In re Geisler* as an example supporting Applicant's argument that Hirose teaches away from the claimed bore size. However, there are notable differences between the cited example and Hirose. The statement 'should not be less than about [100 Angstroms]' does indeed teach away, because it explicitly forbids smaller thicknesses, irrespective of any other considerations. Hirose, on the other hand, states "a radius of the through hole is set to be equal to or smaller than 175 μm and is equal to or greater than 125 μm. ... [W]hen the radius ... is smaller than 125 μm, it is difficult to form the through hole by a drill." In other words, Hirose chose the lower limit of 125 microns because it was difficult to drill smaller holes, not because the method does not function properly with smaller holes if such smaller holes can be drilled. Upon reading Hirose, one of skill in the art would instantly recognize that if one could make smaller through holes, then one could use the process taught by Hirose, because Hirose does not in any way prohibit the use of the method with such through holes. As shown in the Stopperan reference, it is well known

in the art to drill holes of the claimed size by means of a laser. Therefore, the limit given as an example by Hirose is not applicable.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LIVIUS R. CAZAN whose telephone number is (571) 272-8032. The examiner can normally be reached on M-F 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DERRIS H. BANKS can be reached on (571) 272-4419. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. Dexter Tugbang/
Primary Examiner
Art Unit 3729

/L. R. C./ 7/18/2009
Examiner, Art Unit 3729